WHAT IS CLAIMED IS:

1. A multiport data communication system for switching data packets between ports, the data communication system comprising:

a plurality of ports for receiving and transmitting data packets; and

a memory storing the received data packets; wherein

at least some of the ports include

a transmit queue queuing data packets retrieved from the memory for transmission from the port,

an output terminal outputting the data packets, and

a data path connecting the transmit queue and the output terminal, the data path having a gate controlling transferring of data packets in the data path to the output terminal.

2. The system of claim 1, wherein

the data packets form a data frame,

the transmit queue is coupled to the data path such that all data packets in each respective transmit queue are transferred to the data path, and

the gate is responsive to an enable signal to selectively either transfer an entire frame on the data path to the output terminal or block transfer of the entire frame to the output terminal.

3. The system of claim 2, wherein the gate is an AND gate that has a first input that receives data packets and a second input that receives the enable signal.

4. The system of claim 1, wherein the data path comprises circuitry configured to:

empty the transmit queue of the data packets,

section the data packets into nibbles of data, and

provide an assembled data packet to the gate.

5. The system of claim 4, wherein

the data packets form a data frame,

the transmit queue is coupled to the data path such that all data packets in each respective transmit queue are transferred to the data path, and

the gate is responsive to an enable signal to selectively either transfer an entire frame on the data path to the output terminal or block transfer of the entire frame to the output terminal.

6. The system of claim 5, wherein the gate is an AND gate that has a first input that receives data packets and a second input that receives the enable signal.

7. The system of claim 4, wherein the circuitry comprises a plurality of multiplexers.

8. A method in a communication system of controlling transmission of received data packets from at least one of a plurality of transmit ports comprising:

receiving data packets via a plurality of receive ports;

storing the received data packets in a memory;

reading data from the memory corresponding to each data packet to be transmitted from a respective transmit port and storing in a transmit queue for the respective transmit port;

transferring each data packet from the transmit queue to a data path connected between the transmit queue and an output terminal; and

responsive to assertion and deassertion of an enable signal, transferring and blocking transferring data packets in the data path to the output terminal.

9. The method of claim 8, wherein

transferring each data packet from the transmit queue empties the transmit queue of the data packets, and

the data path includes circuitry for

sectioning the data packets into nibbles of data, and

providing an assembled data packet.

10. The method according to claim 8, wherein said enable signal controls an AND gate in the data path.

11. The method according to claim 10, wherein

the data packets comprise frame data,

each data in each respective transmit queue is transferred to the data path irregardless of the assertion or deassertion of the enable signal, and

the enable signal controls the AND gate for one of transferring an entire frame on the data path to the output terminal and blocking transferring the entire frame to the output terminal.

12. A bit bucket arrangement in a data communication switch, comprising:

a transmit queue that queues data received at a first port of the switch for transmission from a second port of the switch;

an output terminal coupled to the second port;

a data path coupled between the transmit queue and the output terminal; and

logic coupled to the data path that selectively controls blocking of data from the transmit queue to the output terminal.

13. The bit bucket arrangement according to Claim 12, wherein the logic is an AND gate.

14. The bit bucket arrangement according to Claim 12, wherein

an entire frame is blocked or not blocked completely.

15. The bit bucket arrangement according to Claim 12, wherein the logic selectively controls blocking of data from the transmit queue to the output terminal in responsive to a control signal generated by control logic.

16. The bit bucket arrangement in a switch according to Claim 13, wherein the data path comprises circuitry configured to:

empty the transmit queue of data,

section the data into nibbles of data, and

provide an assembled data packet to the AND gate.

17. The system of claim 16, wherein the circuitry comprises a plurality of multiplexers.